## REMARKS

Claims 1-13 are pending in the present application. Claims 1-6 have been amended. Claims 7-13 have been presented herewith.

## Priority Under 35 U.S.C. 119

A certified copy of Japanese Priority Application No. 2003-324127 has been filed concurrently herewith. **The Examiner is respectfully requested to acknowledge receipt of the certified copy of the priority document, and to confirm that the Claim for Priority Under 35 U.S.C. 119 is complete**.

## Drawings

The drawings have been objected to as failing to comply with 37 C.F.R. 1.84(p)(4), because reference numerals 204 and 206 in Fig. 6 each denote the same element. The drawings have also been objected to because Fig. 6 shows two different layers denoted by reference numeral 210. Also, the Examiner has required that Fig. 6 be designated as "PRIOR ART".

Enclosed is one (1) red-inked drawing Annotated Sheet, wherein BOX oxide film 204 and SOI layer 206 have been clearly denoted. Also, Fig. 6 has been denoted as "PRIOR ART", as requested by the Examiner. Also enclosed is one (1) drawing Replacement Sheet, incorporating the above noted corrections. **The Examiner is respectfully requested to acknowledge receipt and acceptance of the drawing**

**Replacement Sheet.**

The drawings have also been objected to as failing to comply with 37 C.F.R. 1.84(p)(5), because reference numeral 208 in Fig. 6 is not described in the specification. Responsive to this objection, page 4 of the present application has been amended to identify device-to-device isolation regions 208. The Examiner is therefore respectfully requested to withdraw this objection to the drawings.

## Claim Rejections-35 U.S.C. 103

Claims 1, 2, 4 and 5 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Lin et al. reference (U.S. Patent No. 6,214,722) in view of the Ogure et al. reference (U.S. Patent No. 6,458,694). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

An object of the present application is to reduce the storage of electrical charges developed during metal sputtering or dry etching, which occurs because of a buried insulating layer formed between a support substrate and a silicon layer such as in an SOI wafer for example, to thus prevent reduction in device yield due to charge up. This is a significant problem for SOI wafers, because devices formed in the SOI layer are necessarily electrically floating in view of the buried insulating layer.

The method for manufacturing a semiconductor device of claim 1 includes in combination "removing a layered portion of the intermediate insulating film, the silicon on insulator layer and the buried oxide film provided on a wafer edge region lying

around the wafer, by etching using a resist pattern to thereby expose an edge surface region of the support substrate, which corresponds to the wafer edge region"; and "forming a conductive layer by sputtering so as to cover said exposed edge surface region and the intermediate insulating film". Applicant respectfully submits that the prior art as relied upon by the Examiner does not make obvious these features.

The Examiner has primarily relied upon Figs. 2A – 2F of the Lin et al. reference as meeting the features of the above noted claims. The Examiner has interpreted conductive layer 220, insulating layer 202a and substrate 200 respectively as the conductive layer, the intermediate insulating film and the support substrate of claim 1. The Examiner has however acknowledged that the Lin et al. reference does not disclose any particular method used for depositing conductive layer 220. In order to overcome this acknowledged deficiency, the Examiner has asserted that the Ogure et al. reference teaches that it is advantageous to deposit a metal interconnect layer using a sputtering process, and that it would thus have been obvious to deposit conductive layer 220 in Fig. 2F of the Lin et al. reference by a sputtering process. Applicant respectfully disagrees for the following reasons.

The structure shown in Fig. 2F of the Lin et al. reference as specifically relied upon by the Examiner includes an insulating layer 202a as formed on substrate 200 and as having openings 206a and 206b formed therethrough. A conductive layer 220 is formed on insulating layer 202a and substrate 200, including within openings 206a and 206b. However, the structure in Fig. 2F of the Lin et al. reference does not include a

silicon on insulator layer provided over a buried oxide film. The Lin et al. reference as relied upon by the Examiner therefore does not disclose or make obvious "removing a layered portion of the intermediate insulating film, the silicon on insulator layer and the buried oxide film provided on a wafer edge region lying around the wafer, by etching using a resist pattern to thereby expose an edge surface region of the support substrate, which corresponds to the wafer edge region", as featured in claim 1.

Moreover, the prior art as relied upon by the Examiner fails to recognize that charge incident onto a conductive layer may be caused to flow out of the conductive layer to an exposed edge portion of a support substrate, to thus reduce charge accumulation. This should be clear, because an object of the Lin et al. reference is to perform an interconnection more easily, and to transfer the corresponding pattern more precisely by ensuring an even topography of a wafer surface. The prior art as relied upon by the Examiner, particularly the Lin et al. reference, is not concerned with preventing charge accumulation during sputtering. Accordingly, Applicant respectfully submits that the method for manufacturing a semiconductor device of claim 1 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to claims 1, 2, 4 and 5, is improper for at least these reasons.

Claims 3 and 6 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Lin et al. reference in view of the Ogure et al. reference, in further view of the Wolf et al. reference (Silicon Processing for the VLSI Era: Vol. 1:

Process Technology). Applicant respectfully submits that the Wolf et al. reference as secondarily relied upon by the Examiner does not overcome the above noted deficiencies of the primarily relied upon prior art references. Applicant therefore respectfully submits that claims 3 and 6 would not have been obvious in view of the prior art as relied upon by the Examiner for at least the above reasons.

**Claims 7-13**

The method of manufacturing a semiconductor device of claim 7 includes in combination "providing an SOI wafer as having a substrate, an oxide film on the substrate, and a silicon layer on the oxide film"; "forming a gate element on the silicon layer"; "depositing an insulating layer over the gate element and the silicon layer"; "forming a contact through the insulating layer to the gate element, the contact being exposed at a surface of the insulating layer"; "removing the insulating layer, the silicon layer and the oxide film from an edge region of the SOI wafer, to thereby expose an edge surface region of the substrate"; and "sputtering a conductive layer on the insulating layer, the contact exposed at the surface of the insulating layer, and the edge surface region of the substrate".

As emphasized above, the prior art as relied upon by the Examiner does not disclose an SOI wafer having a substrate, an oxide film on the substrate and a silicon layer on the oxide film, as featured in claim 7. Also, formation of a gate element and a contact are not disclosed in the relied upon prior art. Consequently, the prior art as

relied upon by the Examiner does not disclose or make obvious removing the insulating layer, the silicon layer and the oxide film from an edge region of an SOI wafer as further featured in claim 7. Applicant therefore respectfully submits that claims 7-13 distinguish over and would not have been obvious in view of the prior art as relied upon by the Examiner for at least the above reasons.

## Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

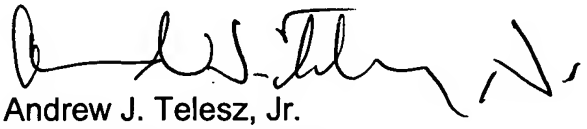
In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

Pursuant to the provisions of 37 C.F.R. 1.17 and 1.136(a), the Applicant hereby petitions for an extension of two (2) months to September 18, 2005, for the period in which to file a response to the outstanding Office Action. The required fee of $450.00 should be charged to Deposit Account No. 50-0238.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.



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Enclosures: One (1) drawing Annotated Sheet
One (1) drawing Replacement Sheet

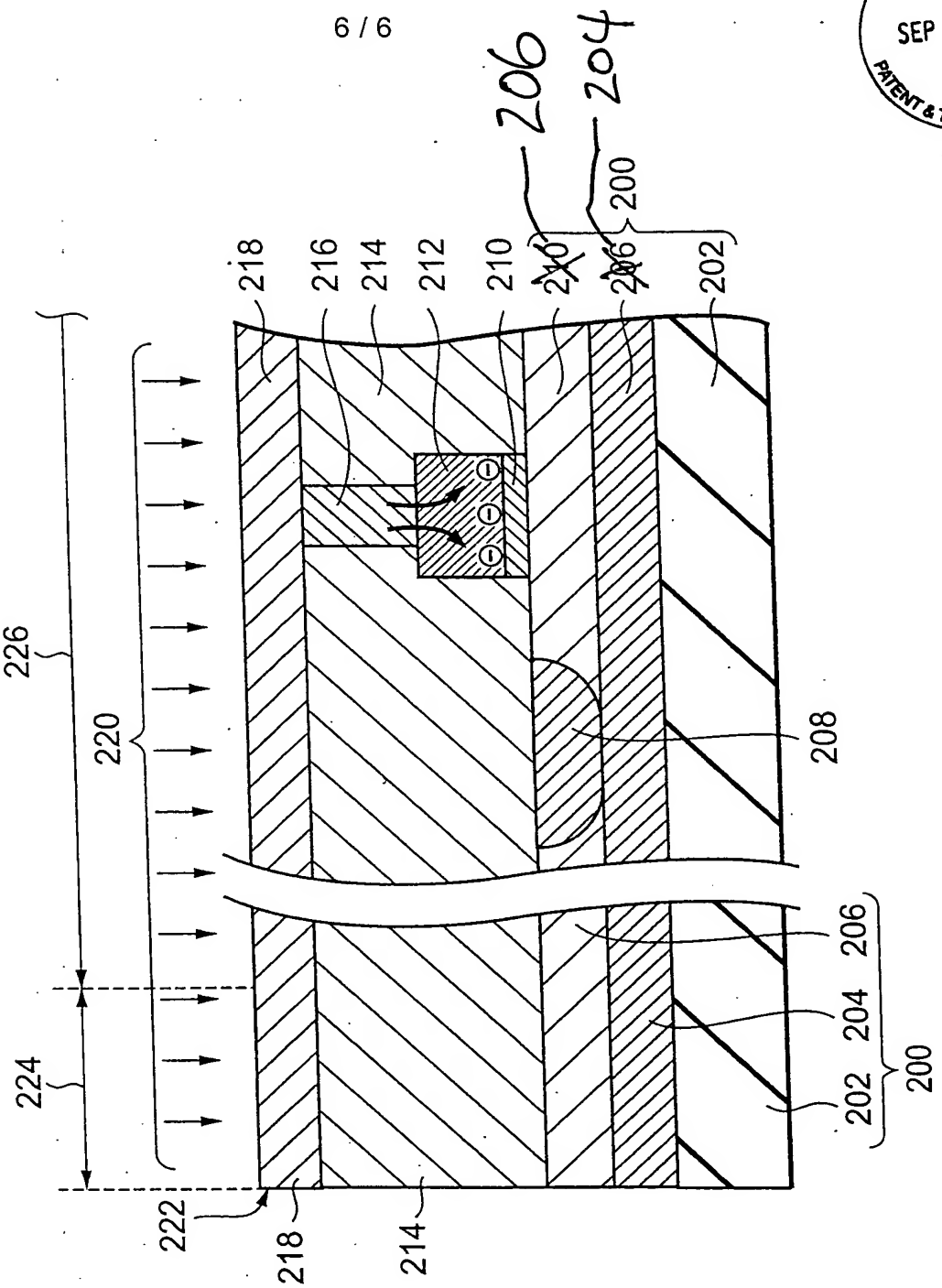


FIG. 6
PRIOR ART